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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SUNG-KYU CHOI

Appeal 2008-4828
Application 10/758,040[1]
Technology Center 2100

Decided:[2] February 25, 2009

Before JOHN C. MARTIN, JEAN R. HOMERE,
and CAROLYN D. THOMAS, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* HOMERE.

Opinion dissenting-in-part and concurring-in-part filed by *Administrative Patent Judge MARTIN.*

HOMERE, *Administrative Patent Judge*.

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[1] Filed on January 16, 2004. The real party in interest is Samsung Electronics Company., Ltd. An Oral Hearing was held on this appeal on February 11, 2009.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 through 10. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

Appellant's Invention

Appellant invented a processor bus connection apparatus for connecting a processor to a dual bus system to separately transfer ordinary data via a synchronous data bus, while transferring display data via an asynchronous data bus. (Spec. 2, ¶ [06]; *id.* 10-11, ¶ [37].) As depicted in Figure 3 and 9, the processor bus connection apparatus (32) includes a multiplexer (321) and a buffer (322), which contains a read unit and a write unit for each type of bus. The processor bus connection apparatus (25) interfaces with the necessary controllers (22, 27) to identify the nature of an incoming request.

As shown in Figure 2, upon receiving a first data, the processor bus connection apparatus (25) transfers the first data received from the processor (21) to a first memory (23) via the synchronous bus. Alternatively, upon receiving a second data from the first memory (23) via the synchronous bus, the processor bus connection apparatus (25) transfers the received second data to the processor (21). (*Id.* at 11-12, ¶¶ [38]-[39].) Upon receiving a third data, the processor bus connection apparatus (25) transfers the third data

received from the processor (21) to a second memory (28) via the asynchronous bus. Alternatively, upon receiving a fourth data from the second memory (28) via the asynchronous bus, the processor bus connection bus (25) transfers it to the processor (21). (*Id.* at 12, ¶ [39].)

Illustrative Claims

Independent claims 1 and 2 further illustrate the invention. They read as follows:

> 1. A buffering apparatus comprising:
>
> an asynchronous data bus write unit which, when control information indicating a request for writing in a buffer connected to an asynchronous data bus not synchronized with a processor is provided by a multiplexer connected to the processor, receives third data from the multiplexer, stores the third data, and transfers the stored third data to a second memory through the asynchronous data bus; and
>
> an asynchronous data bus read unit which, when control information indicating a request for reading from the buffer is provided by the multiplexer, receives fourth data from the second memory through the asynchronous data bus, stores the fourth data, and transfers the stored fourth data to the multiplexer,
>
> wherein the multiplexer receives first data from the processor and transfers the received first data to a first memory through a

synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor.

2. A processor bus connection method comprising:

(a) when address information indicating an address of a first memory connected to a synchronous data bus synchronized with a processor, from the processor is received, receiving first data from the processor and transferring the received first data to the first memory through the synchronous data bus, or receiving second data from the first memory through the synchronous data bus and transferring the received second data to the processor; and

(b) when address information indicating an address of a second memory connected to an asynchronous data bus not synchronized with the processor, from the processor is received, receiving third data from the processor, transferring the third data, storing the transferred third data, and transferring the stored third data to the second memory through the asynchronous data bus, or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Sodos	5,239,651	Aug. 24, 1993
Bourke	5,509,124	Apr. 16, 1996
Masayuki	JP 2000092365	Mar. 31, 2000[3]
Luo	6,265,885	Jul. 24, 2001
Barrenscheen	2003/0084226 A1	May 1, 2003

Rejections on Appeal

The Examiner rejects the claims on appeal as follows:

A. Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Bourke and Barrenscheen.

B. Claims 2 through 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Masayuki and Barrenscheen.

C. Claims 7 through 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Masayuki, Barrenscheen, and Sodos.

D. Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Masayuki, Barrenscheen, and Luo.

[3] See also the translation document, PTO 08-6439, Translated by FLS, Inc., July 2008.

Appellant's Contentions

1. Appellant argues that the combination of Bourke and Barrenscheen does not render independent claim 1 unpatentable. (App. Br. 10-11, Reply Br. 4-7.) All of Appellant's arguments are directed to Barenscheen. Particularly, Appellant argues that the Bus Interface (BI1) disclosed in Barrenscheen is not a "multiplexer" that receives a first data from a processor and transfers the received first data to a first memory through a synchronous data bus. Appellant also argues that the disclosed bus interface does not, alternatively, receive a second data from the first memory through the synchronous bus, and subsequently transfers the received second data to the processor. (App. Br. 10.) Rather, Appellant submits that the bus interfaces (BI1-BI4) are used to connect the data transmission device to the first four buses (BUS1-BUS4), respectively. (*Id.*) Further, Appellant argues that Barrenscheen does not disclose that any of the buses BUS1 and BUS2 is synchronized with the processor, as required by claim 1. (*Id.* at 11.)

2. Appellant argues that the combination of Masayuki and Barrenscheen does not render independent claim 2 unpatentable. (App. Br. 12-15, Reply Br. 7-10.) Particularly, Appellant argues that Masayuki is silent on whether the disclosed buses are synchronous or asynchronous. (App. Br. 12.) According to Appellant, Masayuki's disclosure of directly connecting the image bus to the CPU appears to suggest, at best, that the image bus is synchronized with the CPU. (*Id.* at 13.) However, Appellant

submits that such disclosure is no way indicative that the image bus is an asynchronous data bus not synchronized with the processor. (*Id.*)

Examiner's Findings/Conclusions

1. The Examiner finds that since the bus interface (BI1) disclosed in Barrenscheen receives data from module BU11 and transfers the received data to a first memory module BU12, it teaches the claimed multiplexer, as recited in independent claim 1. (Ans. 17-18.) Further, the Examiner finds that Barrenscheen's disclosure of DMA data writing/reading operations from module BU11 to module BU12 suggest that these modules are synchronized with the BUS1 during the DMA data operations. (*Id.* at 18.) Therefore, the Examiner concludes that Bourke and Barrenscheen are properly combined to render claim 1 unpatentable. (*Id.*)

2. The Examiner finds that Masayuki inherently discloses that the CPU bus is synchronized with the CPU since the CPU directly transfers image data to the recording device via the CPU bus. (Ans. 5, 22.) Further the Examiner finds that Masayuki inherently discloses that the image data bus is not synchronized with the CPU since they are separated by numerous interface logics thereby delaying the transfer of image data from the sensor to the storage device through the image data bus. (Ans. 5, 20-24.)

II. ISSUES

1. Did Appellant show that the Examiner erred in concluding that the combination of Bourke and Barrenscheen renders the claimed invention unpatentable? Particularly, the issue turns on whether the ordinarily skilled artisan would have found that Barrenscheen's disclosure of a bus interface teaches or suggests a multiplexer that transfers data from a processor to a memory, and vice-versa, through a data bus synchronized with the processor, as recited in independent claim 1.

2. Did Appellant show that the Examiner erred in concluding that the combination of Masayuki and Barrenscheen renders the claimed invention unpatentable? Particularly, the issue turns on whether the ordinarily skilled artisan would have found that Masayuki's CPU interaction with the CPU bus and the image data bus teaches or suggests a processor synchronized with a synchronous data bus to transfer data to a first memory, and a processor not synchronized with an asynchronous data bus to transfer data to a second memory, as recited in independent claim 2.

III. FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Barrenscheen

1a. As shown in Figure 2A, Barrenscheen discloses a data transmission unit (DTU) for transmitting via two buses (BUS1, BUS2) data

between a plurality of devices (BU11-BU23) including processors and memory devices. (Barrenscheen 2, ¶¶ [0028]-[0029], [0032]-[0035].)

1b. The DTU can transmit data between the devices autonomously (i.e. without the assistance of the CPU) upon request by one of the devices. (*Id.* ¶ [0032].)

1c. As shown in Figure 4, the DTU includes a plurality of bus interfaces (BI1-BI4), which respectively connect the DTU to the buses (BUS1-BUS4) that link the modules. (*Id.* at 3, ¶ [0040].)

1d. Upon receiving a request from a first module (BU11) to transfer data to a second module (BU12), a first bus interface (BI1) in the DTU transfers the received data to the second module via the first bus (BUS1). Similarly, upon receiving a request from the second module (BU12) to transfer data to the first module (BU11), the first bus interface (BI1) transfers the received data to the first module via the first bus (BUS1). (Fig. 2, 4.)

1e. Upon receiving a request from a third module (BU21) to transfer data to a fourth/fifth module (BU22/BU23), a second bus interface (BI2) in the DTU transfers the received data to the fourth/fifth module via the second bus (BUS2). Similarly, upon receiving a request from the fourth/fifth module (BU22/BU23) to transfer data to the third module (BU21), the second bus interface (BI2) transfers the received data to the third module via the second bus (BUS2). (*Id.*)

Masayuki

2a. Masayuki discloses a signal processing device for preventing the congestion of an image data bus. (Masayuki 6, ¶ [0009].)

2b. As shown in Figure 1, the signal processing device (1) includes an image generator (10) coupled to an image processing circuit (20), which is coupled to an external image memory (32). The image processing device (20) is then connected to an image control circuit (40) coupled to an external image recording device (51). (*Id.* at 7, ¶ [0013].)

2c. Particularly, the image processor (20) includes a sync generator (26) that feeds a synchronization signal to the image generating circuit (10), which in turn outputs a vertical and a horizontal components of the sync signal back to the image controller (22) of the image processing circuit (20). (*Id.* at 8, ¶ [0014].)

2d. The memory controller (22) distributes the received image data to the control circuit (40) via the host interface (31). Further, the memory controller (22) forwards the image data to the image memory (32) via memory interface (27). (*Id.* at 10, ¶ [0020].)

2e. As depicted in Figure 2, the image processing circuit (20) uses an image data bus (33) to transfer image data from the image generating circuit (10) to the image memory (32). (*Id.* at 11-12, ¶¶ [0028]-[0030].)

2f. Similarly, the image processing circuit (20) uses a CPU bus (34) to transfer image data to the control circuit (40). Consequently, the

CPU (41) interfaces with the memory controller (22) of the processing circuit (20) via both the image data bus (33) and CPU bus (34). (*Id.*)

2g. Image data travels from the CPU (41) in the control circuit (40) to the image recording device (51) via a CPU bus (34). (*Id.*)

IV. PRINCIPLES OF LAW

Claim Construction

"[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d at 1312 (internal citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313.

"[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d at 1323.

Obviousness

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1734 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and discussed circumstances in which a patent might be determined to be obvious. *Id.* at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

The Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. at 1739). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162 (citing *KSR*, 127 S. Ct. at 1741).

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. *See In re Kahn*, 441 F.3d at 987-988; *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991); and *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Moreover, in evaluating such references it is proper to take into account not only the specific teachings of the references but also the inferences which one skilled in the art would reasonably be expected to draw therefrom. *In re Preda*, 401 F.2d 825, 826 (CCPA 1968).

V. ANALYSIS

Independent claim 1 recites in relevant part a multiplexer receives data from a processor and transfers the data to a memory through a synchronous data bus synchronized with the processor.

We first consider the scope and meaning of the term "multiplexer," which must be given its broadest reasonable interpretation consistent with Appellant's disclosure, as explained in *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997):

> [T]he PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification.

See also In re Zletz, 893 F.2d 319, 321 (Fed. Cir. 1989) (stating that "claims must be interpreted as broadly as their terms reasonably allow."). Appellant's Specification states the following:

> If the multiplexer 321 receives address information, which indicates the address of the first memory connected to the synchronous data bus synchronized with the processor 31, from the processor 31, the multiplexer 321 receives the first data from the processor 31 and transfers the received first data to the first memory through the synchronous data bus, or receives the second data from the first memory through the synchronous data bus and transfers the received second data to the processor 31. If the multiplexer 321 receives address information, which indicates the address of the second memory connected to the asynchronous data bus not synchronized with the processor 31, from the processor 31, the

> multiplexer 321 receives the third data from the processor 31 and transfers the data to the buffer 322, or receives the fourth data from the buffer 322 and transfers the data to the processor 31.

(Spec. 20-21, ¶ [54].)

Our reviewing court further states, "the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent." *Phillips v. AWH Corp.,* 415 F.3d 1303, 1321 (Fed. Cir. 2005.)

Upon reviewing Appellant's Specification, we fail to find a definition for the term "multiplexer." We therefore construe the cited term consistently with its ordinary meaning as provided in a dictionary. A "multiplexer" generally refers to a hardware circuit for selecting a single output from multiple inputs. It is also defined as a device for funneling several different streams of data over a common communications line.[4]

As set forth in the Findings of Facts section, Barrenscheen discloses a bus interface within a data transmission unit for transferring received data between two modules over a bus. (FF. 1d.) While Barrenscheen's bus interface teaches transferring data between a processor and a storage medium over a bus, the disclosed bus interface is not equivalent to a multiplexer, as defined above. Particularly, the bus interface is not a device for selecting an output from multiple inputs, nor is it a device that funnels multiple data streams over the common communication line. We therefore find that the multiplexer is not limited to the functions recited in the claim.

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[4] Microsoft Press, *Computer Dictionary*, 265 (2nd ed. 1994).

That is, the multiplexer also includes the inherent functions associated with the device as set forth in our definitions above. Thus, since claim 1 recites an apparatus, Barrenscheen's bus interface must also disclose these inherent functions associated with the multiplexer order to for us to sustain the Examiner's finding that the two devices have equivalent structures. However, we find no such equivalency between the two devices. Additionally, we agree with the Examiner that input output interface controller (IOIC) disclosed in Bourke does not teach or suggest the multiplexer, as recited in claim 1. (Ans. 4.) It follows that Appellant has shown that the Examiner erred in concluding that the combination of Bourke and Barrenscheen renders independent claim 1 unpatentable.

Independent claim 2 recites a processor synchronized with a synchronous data bus to transfer data to a first memory, and a processor not synchronized with an asynchronous data bus to transfer data to a second memory.

We begin by broadly and reasonably construing the terms "synchronous" and "asynchronous." Appellant's Specification states the following:

> The synchronous bus and asynchronous bus operate respectively. *That is, while the synchronous bus operates geared to the processor, the asynchronous bus operates irrespective of the clock of the processor.* Accordingly, an apparatus for controlling the synchronous bus and an apparatus for controlling the asynchronous bus need to be prepared respectively. The synchronous bus control apparatus 22 plays a role of permitting the use of the synchronous bus so that a plurality of apparatuses can smoothly use the synchronous

> bus. In the same manner, the asynchronous bus control apparatus 27 plays a role of permitting the use of the asynchronous bus so that a plurality of apparatuses can smoothly use the asynchronous bus.

(Spec. 15, ¶ [43]) (emphasis added).

> A bus control apparatus controls traffic between the processor and the plurality of peripheral apparatuses by classifying data transferred by each peripheral apparatus and data transferred to each peripheral apparatus, so that the data can be smoothly transferred between the processor and the peripheral apparatuses. *When the processor communicates data with the peripheral apparatuses through the bus, control information and address information are transferred and received based on the clock of the processor and therefore the processor, the bus, the bus control apparatus, and the peripheral apparatuses should be synchronized with the clock.* According to the present invention, in order to reduce the burden on the bus and to operate irrespective of the clock of the processor, the second memory or the output apparatus is connected to the asynchronous data bus which is not synchronized with the processor. Whether data is transferred through the synchronous data bus or the asynchronous data bus is determined by the destination of the data, that is, the address information which is output from the processor.

(*Id.* at 20, ¶ [53]) (emphasis added).

Upon reviewing Appellant's Specification, we find that the term "synchronous" is defined as "being based upon the clock of the processor". Similarly, we find that the term "asynchronous" refers to "not being based on the processor's clock". Therefore, we interpret the limitation of a "synchronous bus synchronized with the processor" as being a bus that follows the clock of the processor to receive and transfer incoming data.

Conversely, we construe the limitation of an "asynchronous bus not synchronized with the processor" as being a bus that does not follow the clock of the processor to receive and transfer incoming data.

As detailed in the Findings of Fact section above, Masayuki discloses an image data bus that receives synchronization signal components from an image generator to subsequently distribute such signal to numerous devices including a CPU, an image memory device, and a recording device. (FF. 2c-2e.) Masayuki also discloses a CPU bus that allows the processing circuit to directly communicate with the control circuit, which includes a CPU, and a recording device. (FF. 2f-2g.) While the cited disclosure of Masayuki teaches transferring data between a processor and storage media by using different buses, it is silent as to how the clock of the processor relates to the buses. We find nothing in the record before us to clearly support the Examiner's finding that the image data bus is asynchronous, and that the CPU bus is synchronous. Instead, the Examiner inappropriately corresponds Masayuki's disclosure of a sync signal directed to the image data bus as an indication that the bus is inherently asynchronous. However, we find that this disclosure appears to have no bearing on the clock of the disclosed processor. Even if the Examiner's interpretation of the synch signal were correct, at most it would only go to show that the image data bus is synchronous (not asynchronous as asserted by the Examiner). We do not readily find in Masayuki's disclosure any discussion or suggestion of whether or not the cited buses follow the clock of the processor to transfer

data in the signal processing system. Further, we find no evidence to support the Examiner's finding of inherency. We therefore cannot sustain the Examiner's finding that the image bus is inherently asynchronous to the CPU. We also cannot sustain the Examiner's finding that the CPU data bus is inherently synchronized with the CPU. Additionally, we find that Barrenscheen does not cure the noted deficiencies in Masayuki. It follows that Appellant has shown that the Examiner erred in concluding that the combination of Masayuki and Barrenscheen renders claim 2 unpatentable.

Because claims 3 through 10 also recite the synchronous and asynchronous data bus limitation, and the tertiary references relied upon do not cure the deficiencies of the Mayasuki-Barrenscheen combination, Appellant has also shown error in the Examiner's rejections of those claims.

VI. CONCLUSION OF LAW

Appellant has shown that the Examiner erred in concluding that claims 1 through 10 are unpatentable as set forth above.

VII. DECISION

We reverse the Examiner's decision to reject claims 1 through 10.

REVERSED

MARTIN, *Administrative Patent Judge,* dissenting-in-part and concurring-in-part.

I write separately because I respectfully dissent from the Majority's decision to reverse the rejection of claim 1. Also, while I agree with the Majority's decision to reverse the rejection of the other claims, I believe it is necessary to address a point not addressed by the Majority in the discussion of the rejection of claim 2.

Claim 1

I agree with the Majority that because the claim term "multiplexer" is not defined in Appellant's Specification, it must be given its broadest reasonable interpretation consistent with Appellant's disclosure. *In re Thrift*, 298 F.3d 1357, 1364 (Fed. Cir. 2002). However, for the following reasons, I do not agree that "multiplexer" should be given the dictionary definition cited by the Majority, i.e., a hardware circuit for selecting a single output from multiple inputs or a device for funneling several different streams of data over a common communications line. Microsoft Press, *Computer Dictionary* 265 (2d ed. 1994).

The Examiner found that the definition of "multiplexer" in *Merriam-Webster's Collegiate Dictionary* (10th ed.) as "being or relating to a system, of transmitting several messages or signals simultaneously on the same circuit or channel" is inconsistent with the Specification, in which, the Examiner found, "the claimed subject matter 'multiplexer' is no more specific [a] component than *an interfacing component* among processor,

buffer, synchronous data bus, and asynchronous data bus, in the specification, page 20, paragraphs [54]-[55], and Figs. 3-4." Answer 18 (emphasis added). For this reason, the Examiner construed the "wherein" clause of claim 1, which specifies that "the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor," as broad enough to read on Barrenscheen's bus interface BI1, which the Examiner found performs the claimed functions.

In my view, the Examiner's construction of "multiplexer" comports with the principle that it is appropriate to "rely on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or *ascertained by a reading of the patent documents*." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1322-23 (Fed. Cir. 2005) (emphasis added) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584 n.6 (Fed. Cir. 1996)). I understand the Examiner's position to be that the apparent inconsistency between the dictionary definition of "multiplexer" and the functions of the "multiplexer" in Appellant's disclosure suggests that Appellant applied the term "multiplexer" to the disclosed apparatus because it is used to transfer data back and forth between various components in the claimed manner without

regard to whether the disclosed apparatus also satisfies a dictionary definition of that term.

For the foregoing reasons, the Examiner, in my view, has prima facie established that the dictionary definition of "multiplexer" does not apply to the claims, thereby shifting the burden to Appellant to show that the Application describes the disclosed "multiplexer" as being capable of performing the functions set forth in the dictionary definition (in addition to performing the claimed functions, which are described). Because Appellant has not made such a showing, I would affirm the rejection of claim 1.

Claim 2

As noted by the Majority, the Examiner found that Masayuki's image data bus 33 and CPU bus 34 are inherently asynchronous and synchronous, respectively. The Majority's decision that Appellant has shown that the Examiner erred in finding that image data bus 33 is inherently asynchronous addresses only the Examiner's reliance on sync generator 26, which is addressed at page 18 of the Majority opinion. However, the Examiner gave the following additional reason for finding that bus 33 is inherently asynchronous:

> Masayuki uses several interface logics, i.e., Memory Interface 27, Host Interface 31, and JPEG Interface 30 in Fig. 1, between said image data bus and said CPU bus, which are not necessarily required in the Masayuki invention if said image data bus is synchronized with said CPU. In other words, said several interface logics are needed for interfacing between said image data bus and said CPU because said image data bus is not synchronized with said CPU, which is clearly teaching the

> claimed limitation "an asynchronous data bus not synchronized with the processor."

Answer 21. In the absence of any evidence cited by the Examiner to the contrary, I am persuaded by Appellant's argument that "the state of a bus - whether it is synchronous or asynchronous - has nothing to do with whether interfaces are connected between the bus and a CPU." Reply Br. 8.

Because the Examiner has failed to show that image data bus 33 is inherently asynchronous, it is not necessary to address the Examiner's reasons for concluding that CPU bus 34 is inherently synchronous. Answer 22.

> I also note in passing that Appellant is incorrect to argue that
>
> the principle of inherency is applicable only with respect to 35 U.S.C. §102 rejections. Inherency and obviousness are distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. In deciding that a novel combination would have been obvious, there must be a supporting teaching in the prior art; for that which may be inherent is not necessarily known, and obviousness cannot be predicated on what is unknown. *See In re Newell*, 13 U.S.P.Q.2d 1248, 1250 (Fed. Cir. 1989).

Br. 14. *Newell* stands for the proposition that obviousness cannot be based on inherency that was not known. I understand the Examiner's position to be that a person skilled in the art would have recognized that image data bus 33 and CPU bus 34 are asynchronous and synchronous, respectively.

msc

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